

VER : 1A

ZQ2B SOLE UMA SYSTEM DIAGRAM



Danube Platform
(Main Stream)

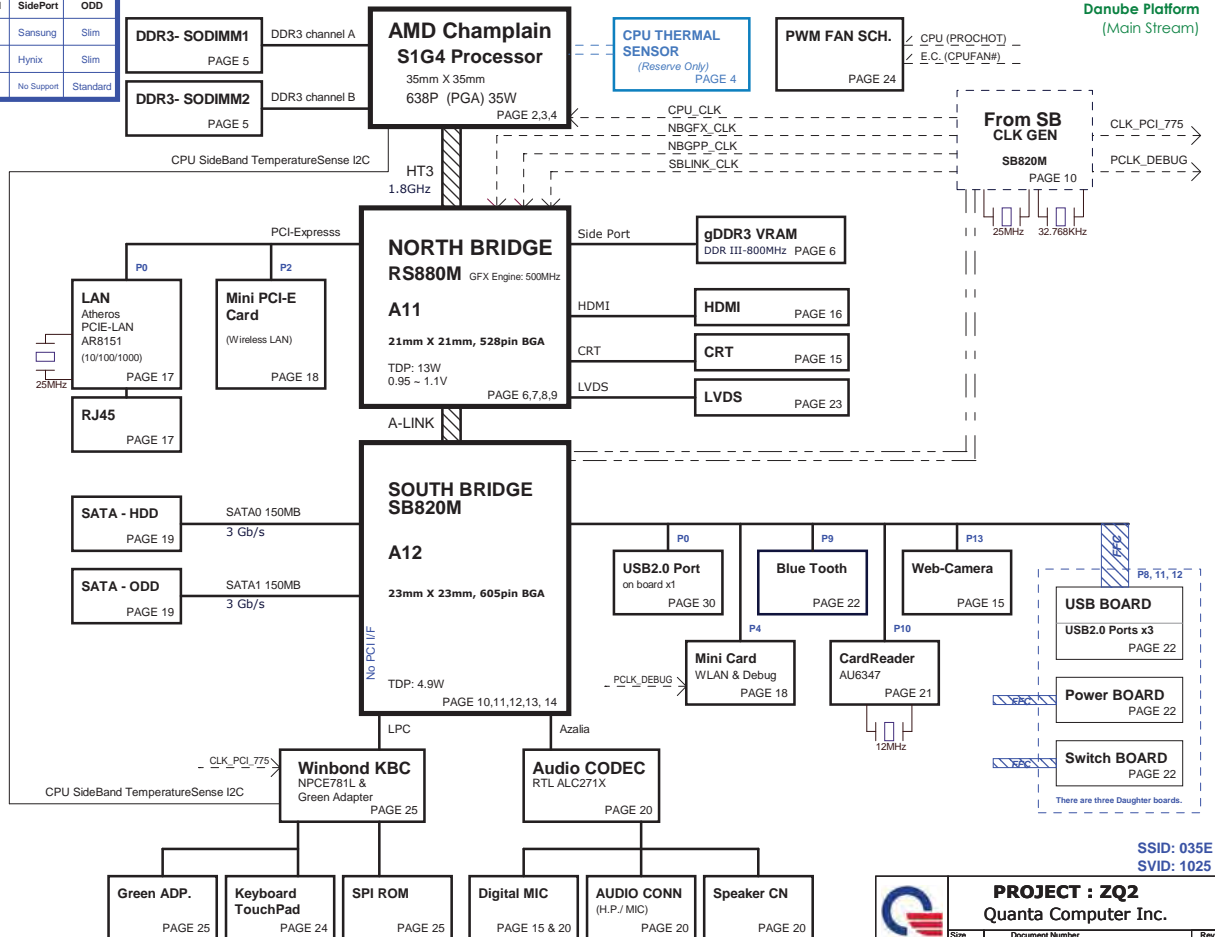
BOM P/N	Description	Model	SidePort	ODD
31ZQ2MB00A0	ZQ2B 6L JM MB (W/GRN,SAM,W/O CPU)ASSY	JM	Samsung	Slim
31ZQ2MB00E0	ZQ2B 6L JM MB (W/GRN,HYU,W/O CPU)ASSY	JM	Hynix	Slim
31ZQ2MB00H0	ZQ2B 6L JV MB (W/GRN,W/O CPU,VRAM)ASSY	JV	No Support	Standard

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

IV @ -----> iGPU
SP @ -----> Option Notice
SIDE @ -----> SidePort VRAM
GA @ -----> Green Adapter (Default stuff)

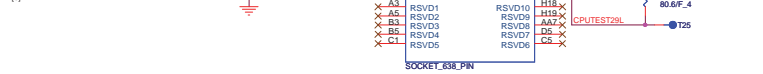
Sideport-L75,L76,R583,R392,C832,R455,R550,R502
NB A11-R105,R108
SB A12-R267,R271
JV/JM-CN16,R450,R456
EC-D8,D27
UMA-R461
VRAM-R358,R359,R360,R363,R365,R72



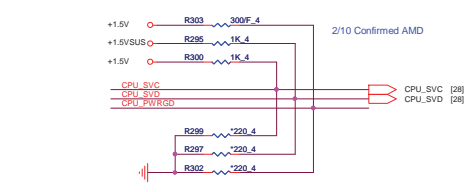
PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	1A
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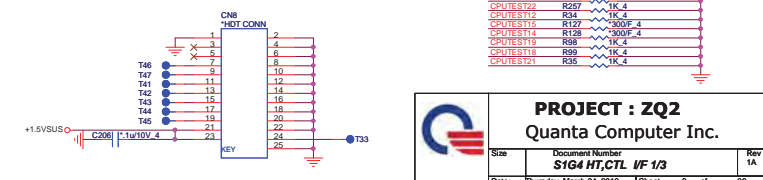
S1G4 (CPU)



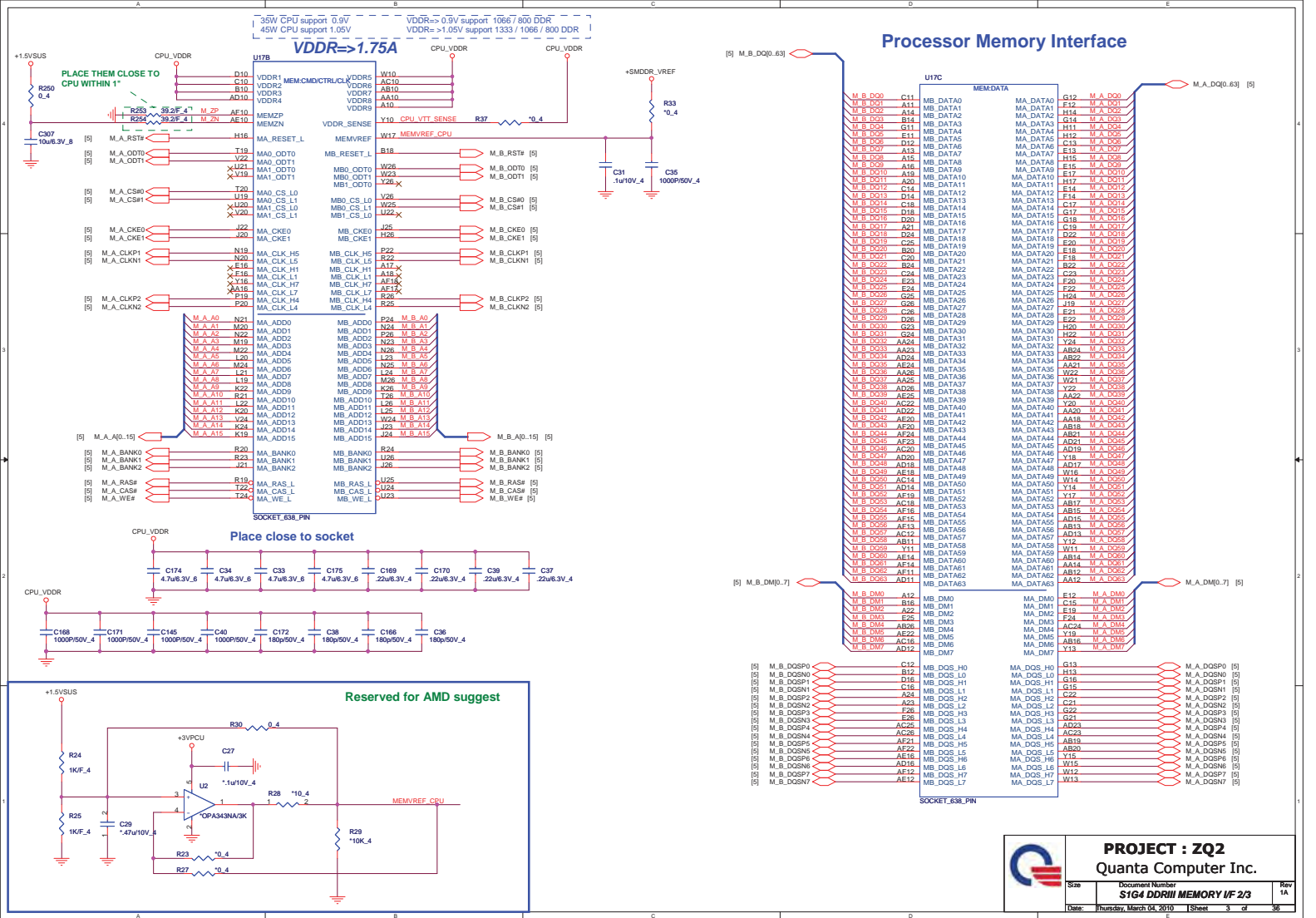
Serial VID

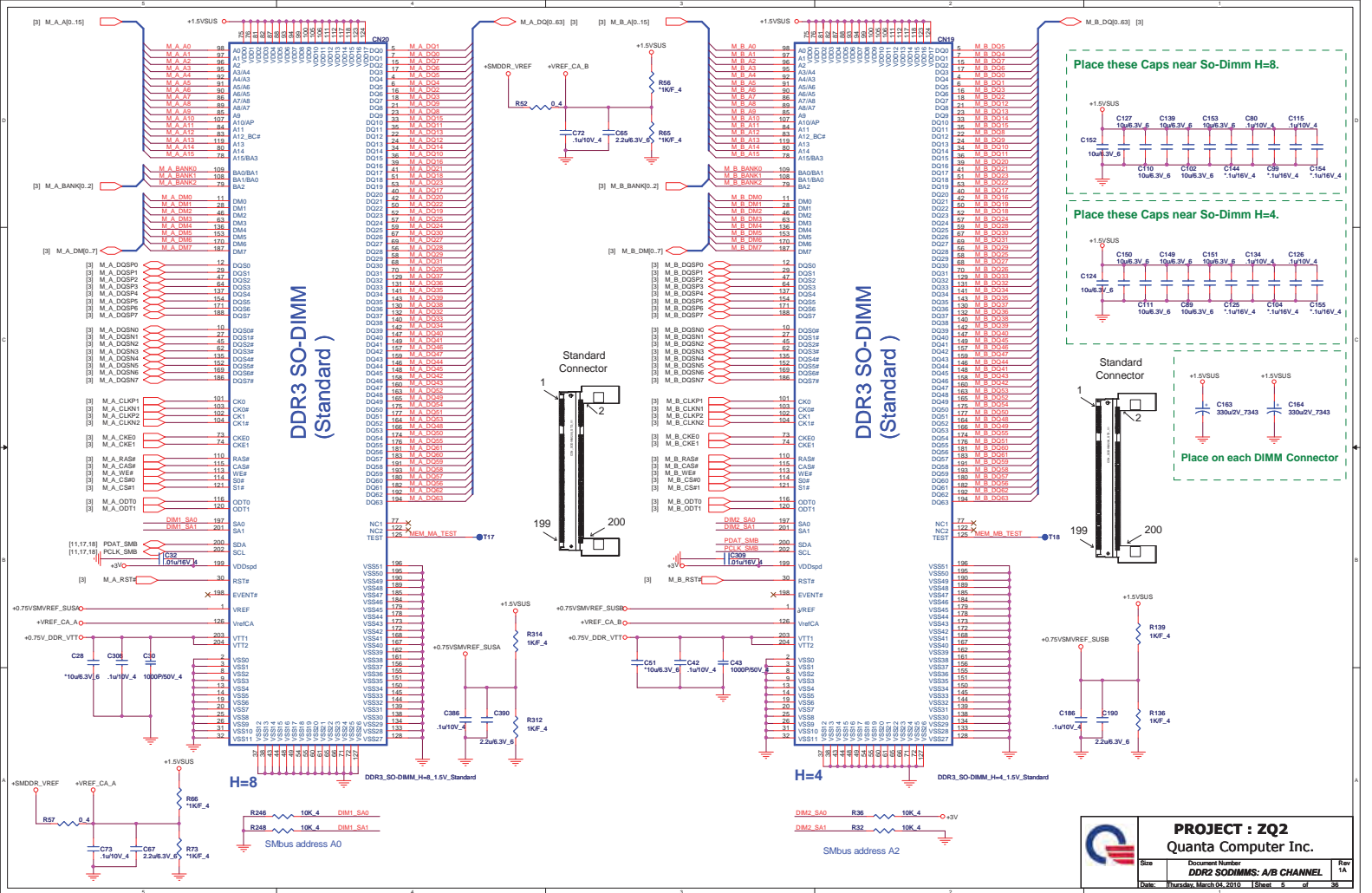


HDT Connector

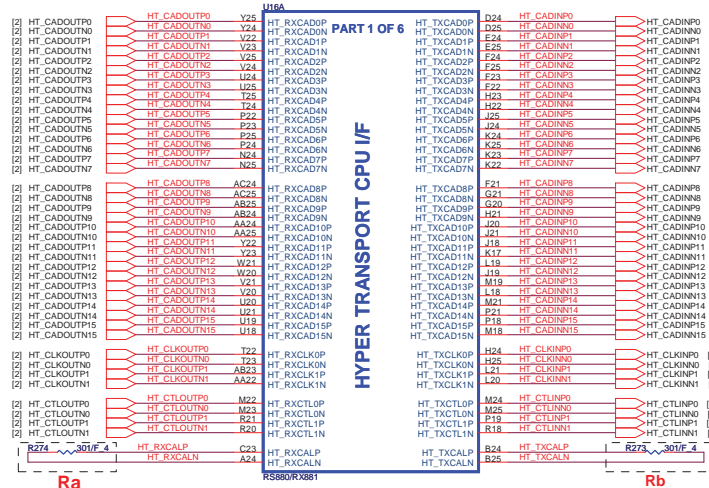
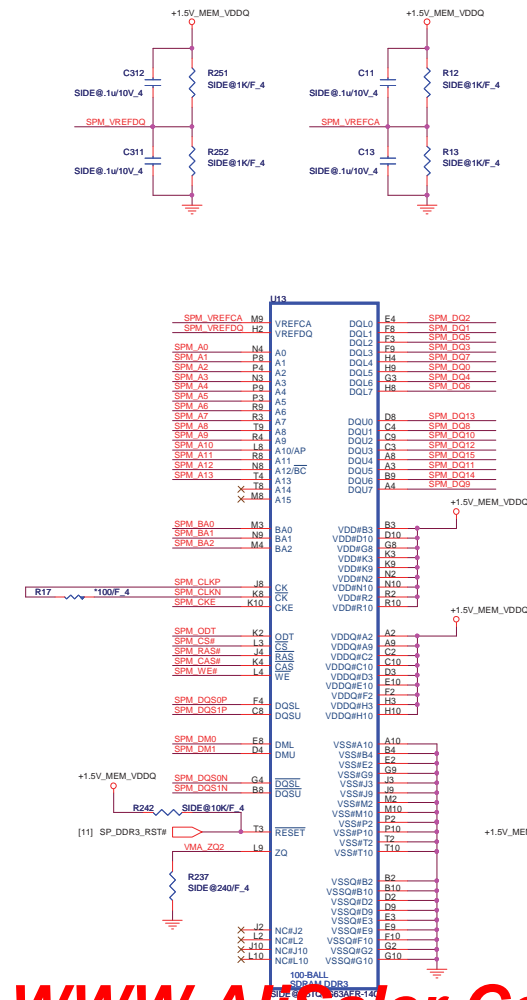


VFIX MODE		VID Override Circuit
SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V





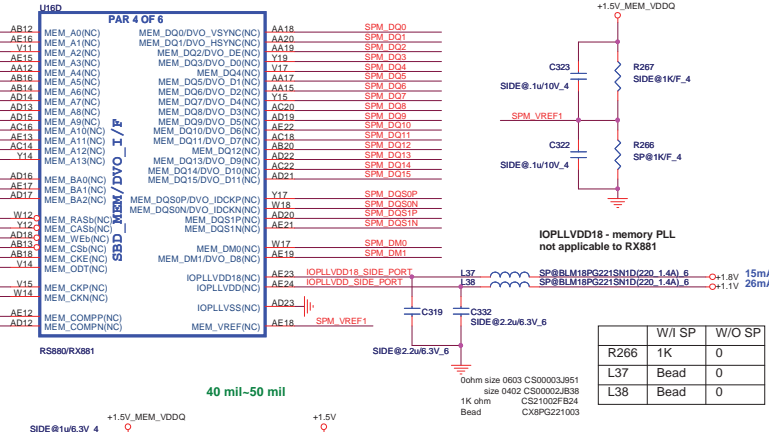
SIDE PORT



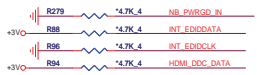
This block is for Side-Port only

Signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +1% (0402)
P/N: CS21212F18



For Check list JTAG



For A11 version

(02/10) Don't need 49.9 ohm PD.



STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO.

RS880M	
1 Disable	<input checked="" type="checkbox"/>
0 Enable	<input type="checkbox"/>



RS880M: Enables Side port memory

RS880M:INT_CRT_HSYNCK

Selects if Memory SIDE PORT is available or not

1 = Memory Side Port Not available

0 = Memory Side port available

Register Readback of strap: NB_CLKCFG.CLK_TOP_SPARE_D[1]



For external EEPROM Debug only

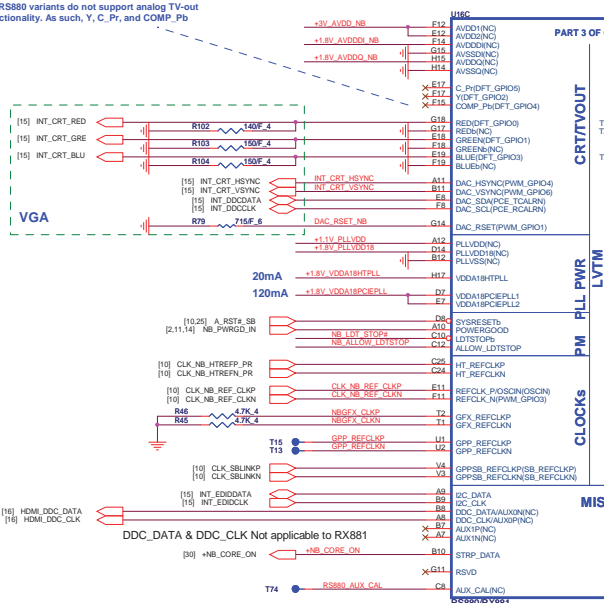
RS780/RX780/RS880

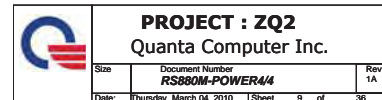


Display Port interface from PCIeGraphics (RS880/rs880M only)

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All RS880 variants do not support analog TV-out functionality. As such, Y, C, Pr, and COMP_Pb





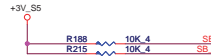
NC only ,Can't be install



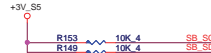
SCL0/SDATA0 is 3V tolerance. AMD datasheet define it
Clk Gen/ Robson/ TV tuner/ DDR2/ Thermal/ Accelerometer



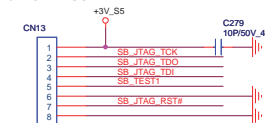
SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it



SCL2/SDATA2 is 3V/S5 tolerance.
AMD datasheet define it

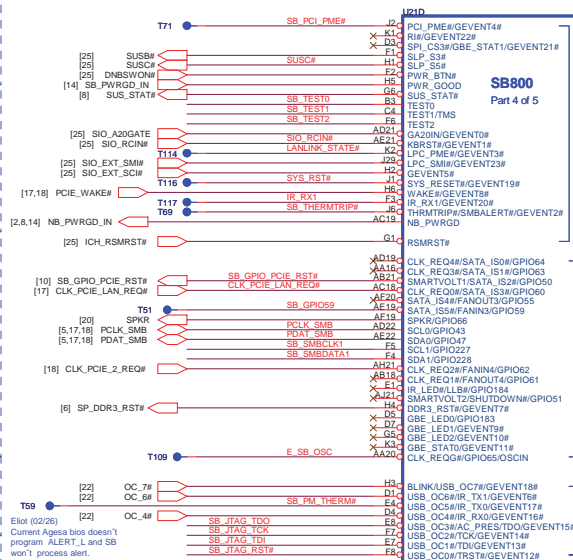
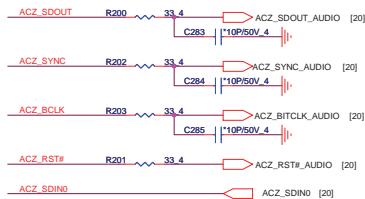


JTAG DEBUG

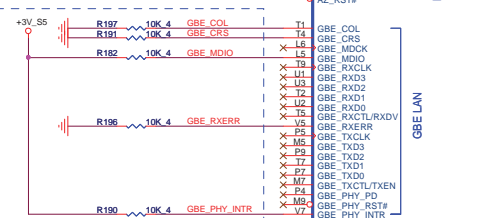
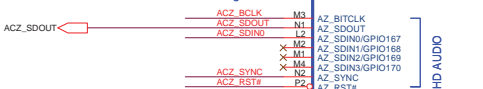


*SW JTAG DEBUG

To Azalia



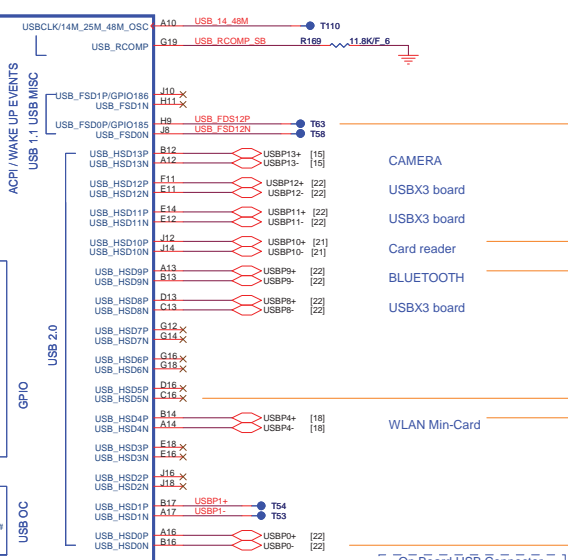
HD audio interface is +3VS5 voltage



[02/22] AMD FAE and checklist request PL.

SB800 A11

USBCLK/41M_25M_48M_OSC pin is CLK input pin when EXT_CLKGEN mode.
It is output CLK source when INT_CLKGEN mode.



CAMERA
USBX3 board
USBX3 board

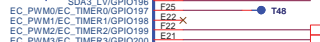
Card reader
BLUETOOTH
USBX3 board

WLAN Min-Card

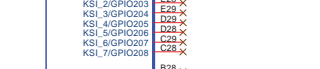
On Board USB Connector

Only USB Port0 can be configured as debug port.

HD AUDIO



EC_PWM1EC_TIMER0/GPIO198
EC_PWM1EC_TIMER1/GPIO199
EC_PWM1EC_TIMER2/GPIO199
EC_PWM1EC_TIMER3/GPIO200



PS2_DAT/S044/GPIO187
PS2_CLK/S044/GPIO188
SPI_CS2/GBE_STAT2/GPIO166
FS_RST/GPIO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

EMBEDDED CTRL

EMBEDDED CTRL

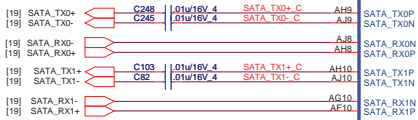
Check list



PROJECT : ZQ2
Quanta Computer Inc.

Max trace length: 6"

SATA HDD

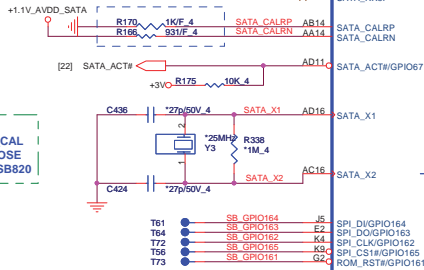


SATA ODD

SATA PORT 0,1,2,3 can support AHCI mode

Signal Name	Explanation
SATA_CALRP	SB800 A11: 800 ohm 1% resistor to GND. SB800 A12: 1K ohm 1% resistor to GND.
SATA_CALRN	SB800 A11: 931 ohm 1% resistor to VDDAN_11_SATA. SB800 A12: 931 ohm 1% resistor to VDDAN_11_SATA.

E-SATA

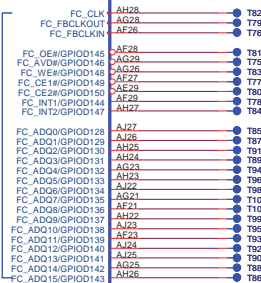


PLACE SATA CAL RES VERY CLOSE TO BALL OF SB820

SB800 A11

SB800
Part 2 of 5

FLASH



SERIAL ATA

HW MONITOR

SPI ROM

BT OFF#

WLAN_DET#

CRD_REQ#

TEMPIN0

TEMPIN1

MB_THRMDA_SB

SB_GPIO174

TEMP_COMM

SB_GPIO175

SB_GPIO176

SB_GPIO177

SB_GPIO178

SB_GPIO179

SB_GPIO180

SB_GPIO181

SB_GPIO182

SB_GPIO183

SB_GPIO184

SB_GPIO185

SB_GPIO186

SB_GPIO187

SB_GPIO188

SB_GPIO189

SB_GPIO190

SB_GPIO191

SB_GPIO192

SB_GPIO193

SB_GPIO194

SB_GPIO195

SB_GPIO196

SB_GPIO197

SB_GPIO198

SB_GPIO199

SB_GPIO200

SB_GPIO201

SB_GPIO202

SB_GPIO203

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SB_GPIO397

SB_GPIO398

SB_GPIO399

SB_GPIO400

SB_GPIO401

SB_GPIO402

SB_GPIO403

SB_GPIO404

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SB_GPIO406

SB_GPIO407

SB_GPIO408

SB_GPIO409

SB_GPIO410

SB_GPIO411

SB_GPIO412

SB_GPIO413

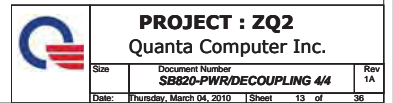
SB_GPIO414

SB_GPIO415

SB_GPIO416

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

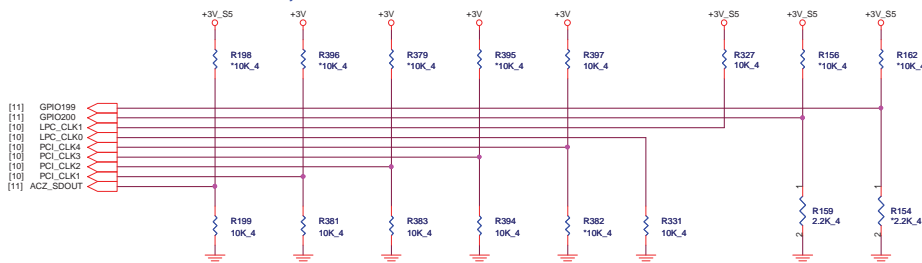
VDD-- S/B CORE power



REQUIRED STRAPS

SB820M is supported Gen.1 mode only.

For internal clock GEN.

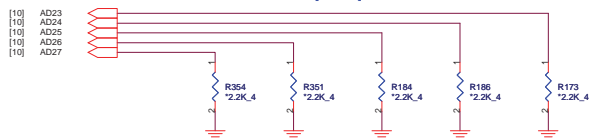


	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L, H=LPC ROM L, L=FWH ROM	

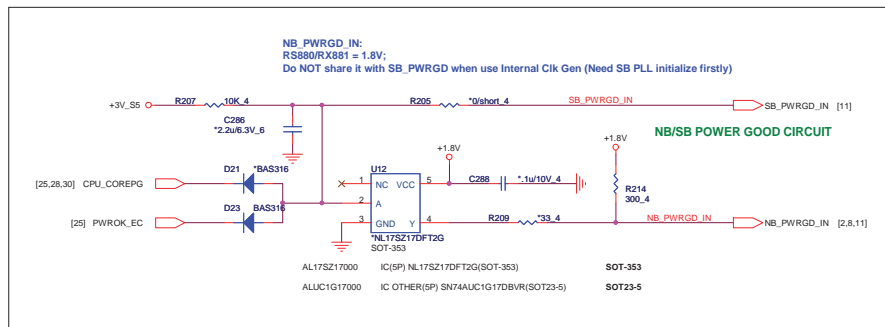
internal have pull Hi 10K

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



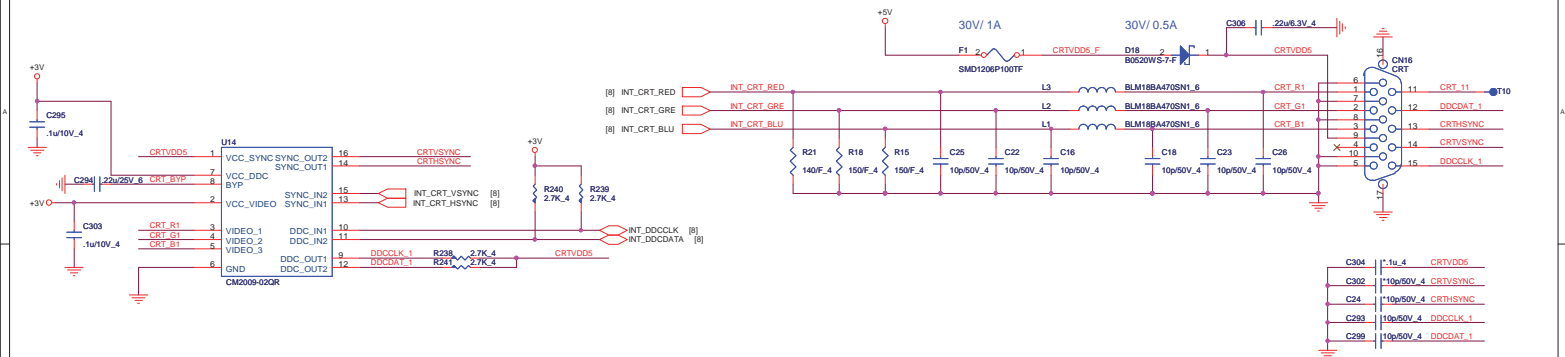
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



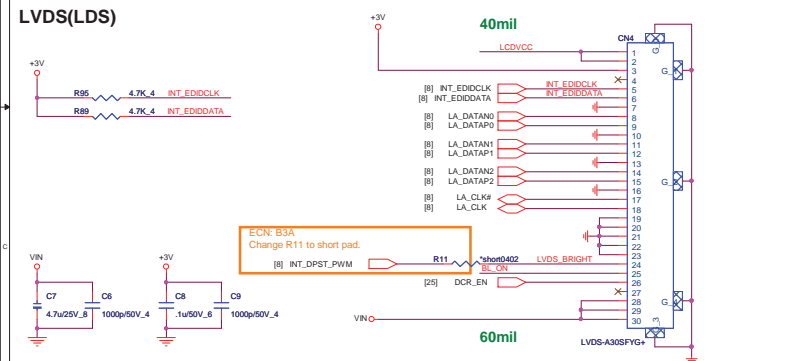
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



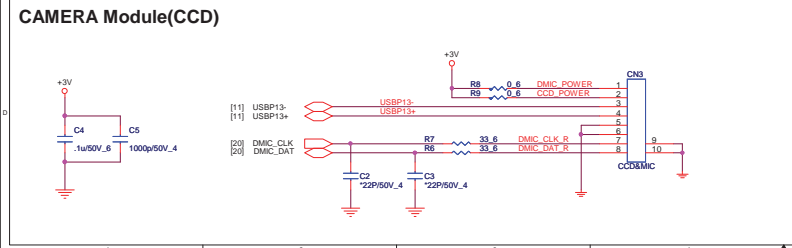
CRT



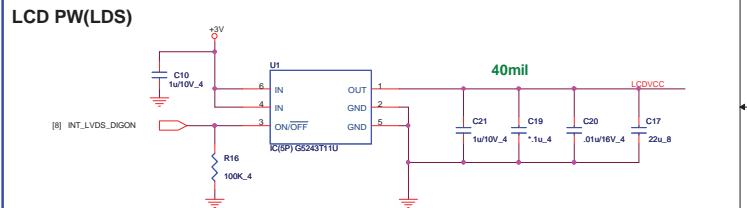
LVDS(LDS)



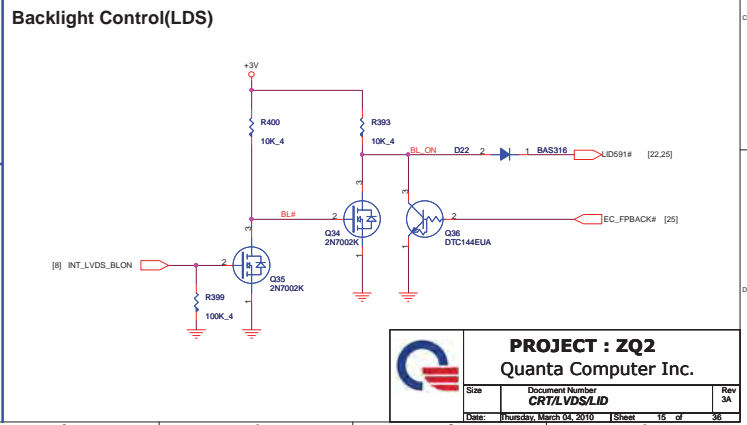
CAMERA Module(CCD)



LCD PW(LDS)



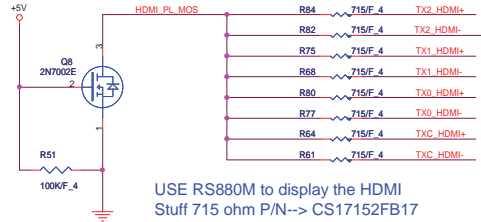
Backlight Control(LDS)



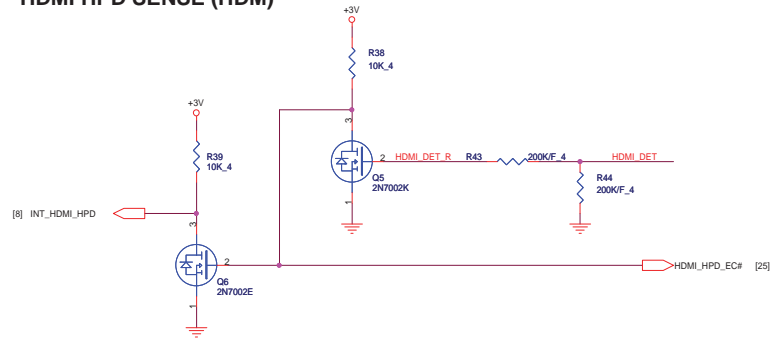
HDMI (HDM)



Close to HDMI Connector



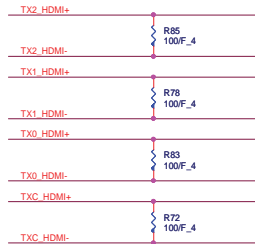
HDMI HPD SENSE (HDM)



HDMI PORT (HDM)

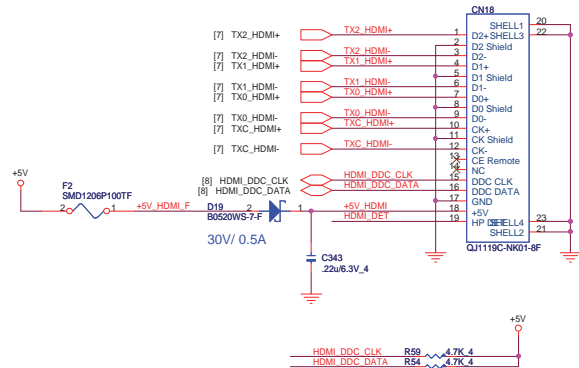
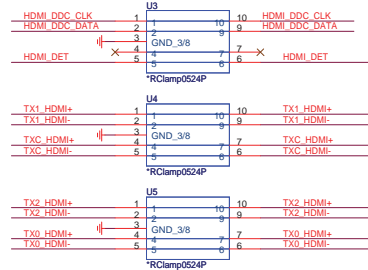
EMI reserve for HDMI(EMC)

Close connector

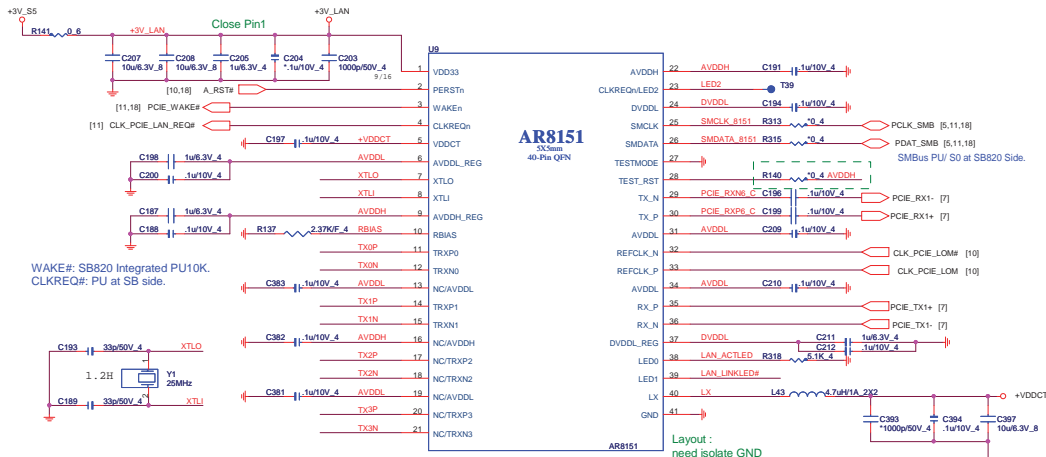


ESD Protect (EMC)

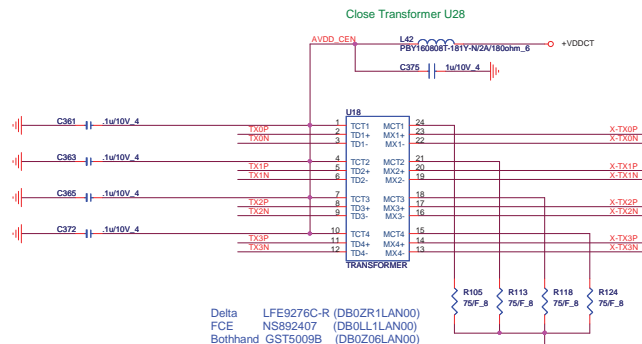
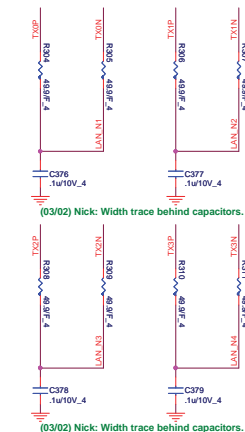
close to HDMI connector



Giga-LAN AR8151

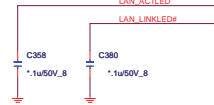
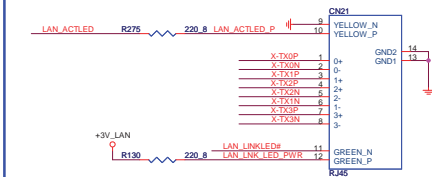


TRANSFORMER(LAN)



Delta	LFE9276C-R (DB0ZR1LAN00)
FCE	NS892407 (DB0LL1LAN00)
Bothhand	GST5009B (DB0Z06LAN00)

RJ45(LAN)



Sertek (03/01):
EMI capacitors, 470pF is enough.
Don't over 490 pF.

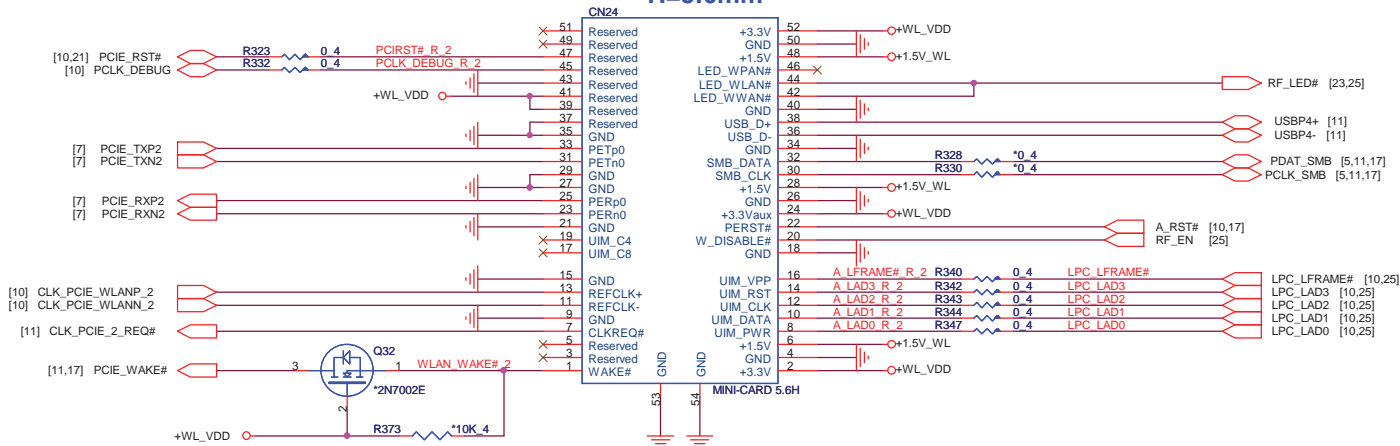


PROJECT : ZQ2
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MINI-CARD WLAN(MNC)

H=5.6mm



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Quanta Computer Inc.

Size	Document Number	Rev
	Mini-Card/WL	1A
Date:	Thursday, March 04, 2010	Sheet 18 of 36



1

1



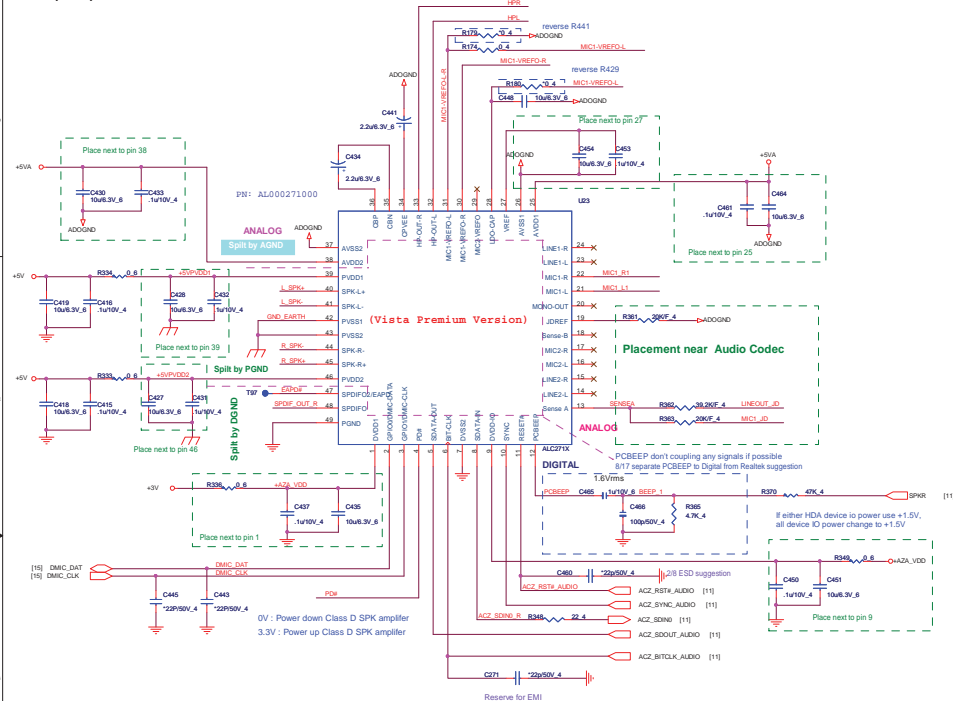
D

D

Main	DFHS13FR017
Second	DFHS13FR006, DFHS13FR005

[illegible]

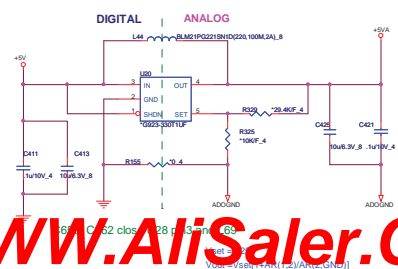
Codec(ADO)



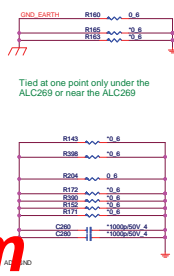
Power (ADO)

Demodulation Filter

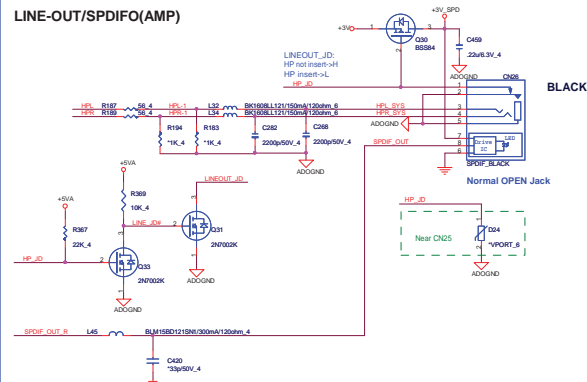
BEAD place close to CODEC.



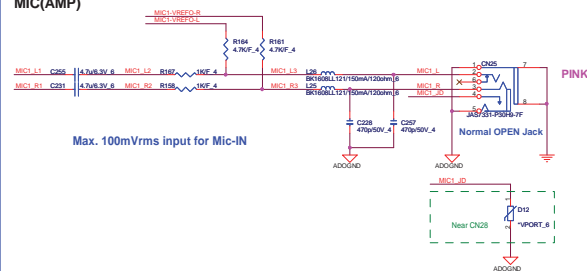
GND_EARTH don't coupling AGND and SPK signals



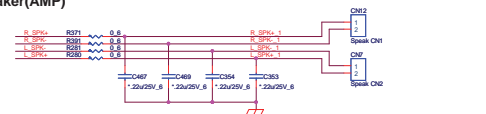
LINE-OUT/SPDIFO(AMP)



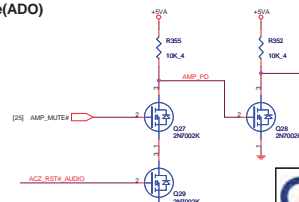
MIC(AMP)



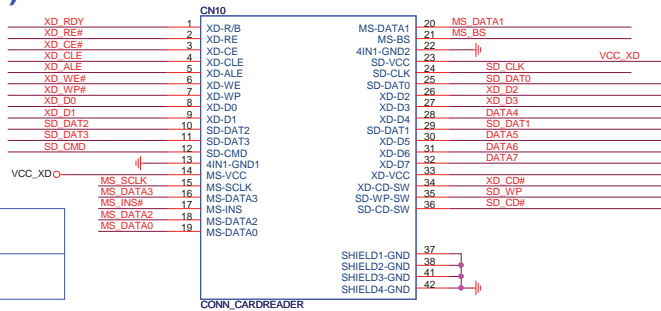
Internal Speaker(AMP)



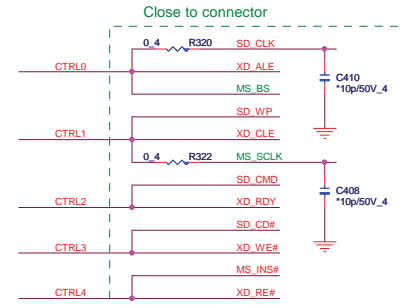
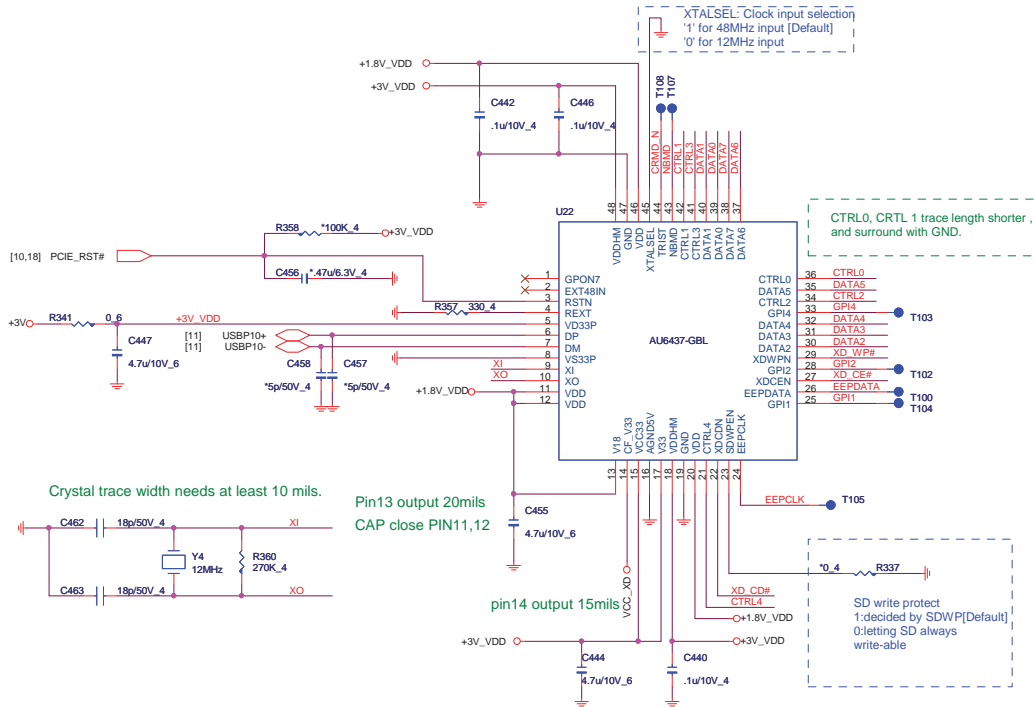
Mute(ADO)



Main	??
Second	??



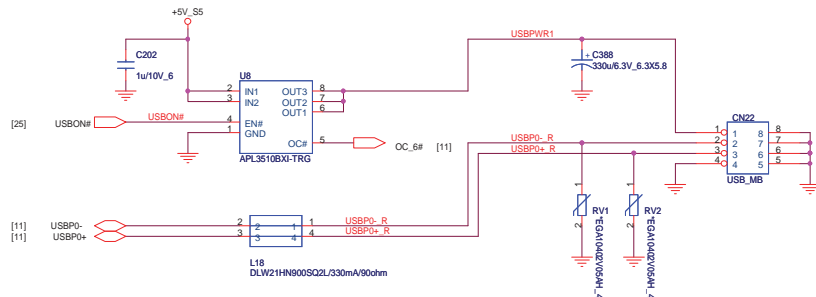
The diagram shows four data inputs (DATA0, DATA1, DATA2, DATA3) connected to SD inputs (SD_DAT0, SD_DAT1, SD_DAT2, SD_DAT3) and MS inputs (MS_DATA0, MS_DATA1, MS_DATA2, MS_DATA3). Each data input is connected to its corresponding SD and MS inputs.



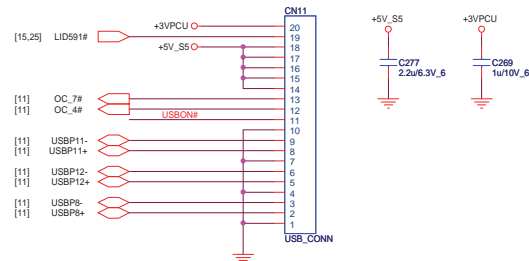
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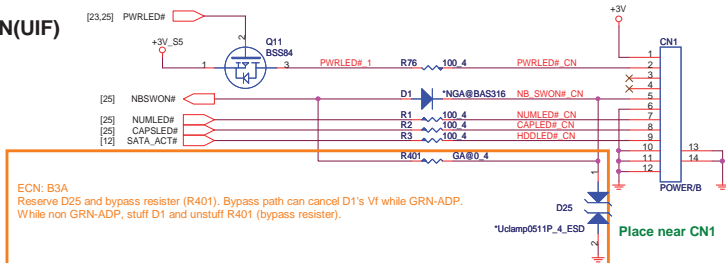
USB PORT(USB/MB)



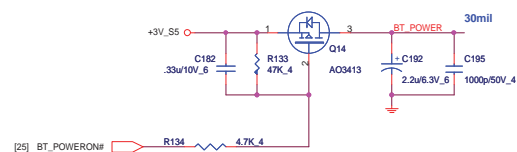
USB BOARD CONN(USB/SB)



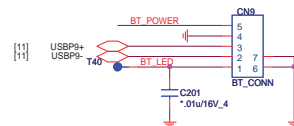
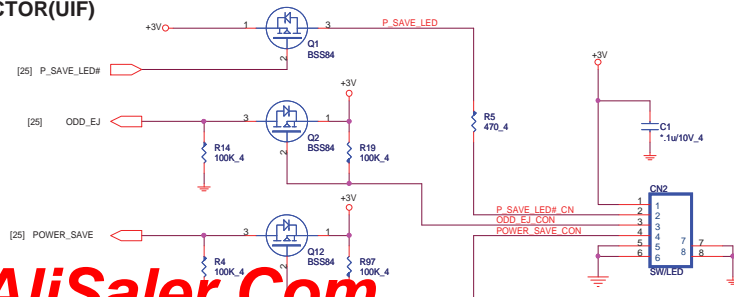
POWER BOARD CONN(UIF)



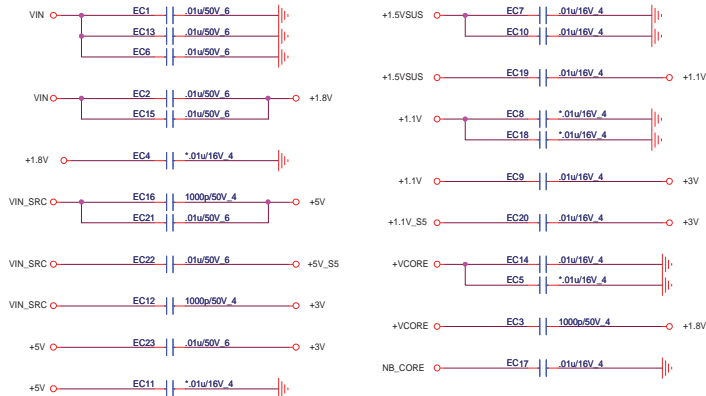
BLUETOOTH CONN(BTM)



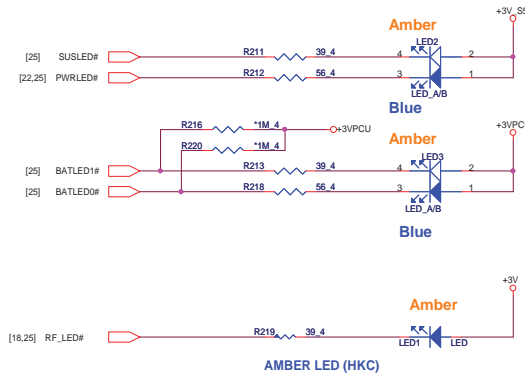
LED BOARD CONNECTOR(UIF)



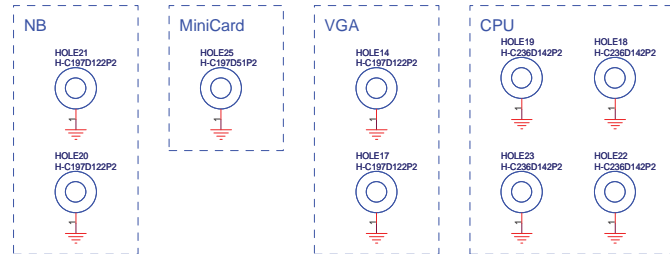
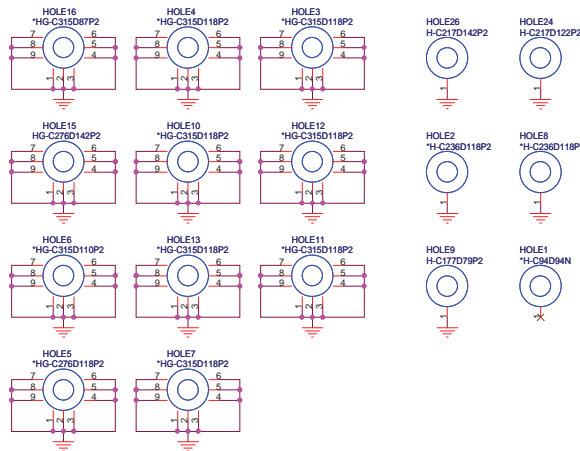
EE RETURN-PATH CAPACITORS(EMC)



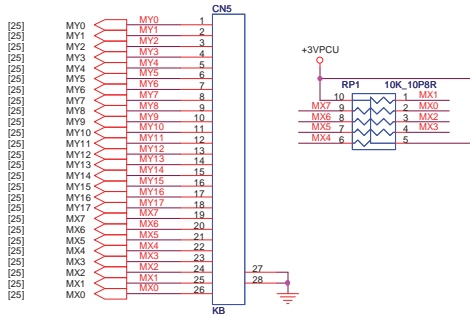
LED(UIF)



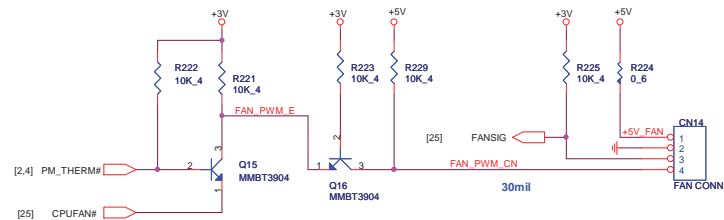
HOLE(OTH)



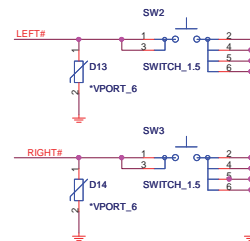
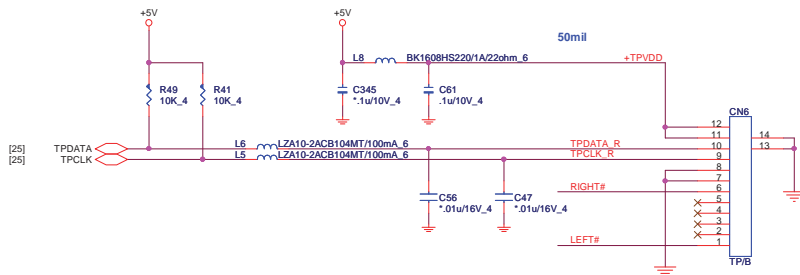
K/B(KBC)



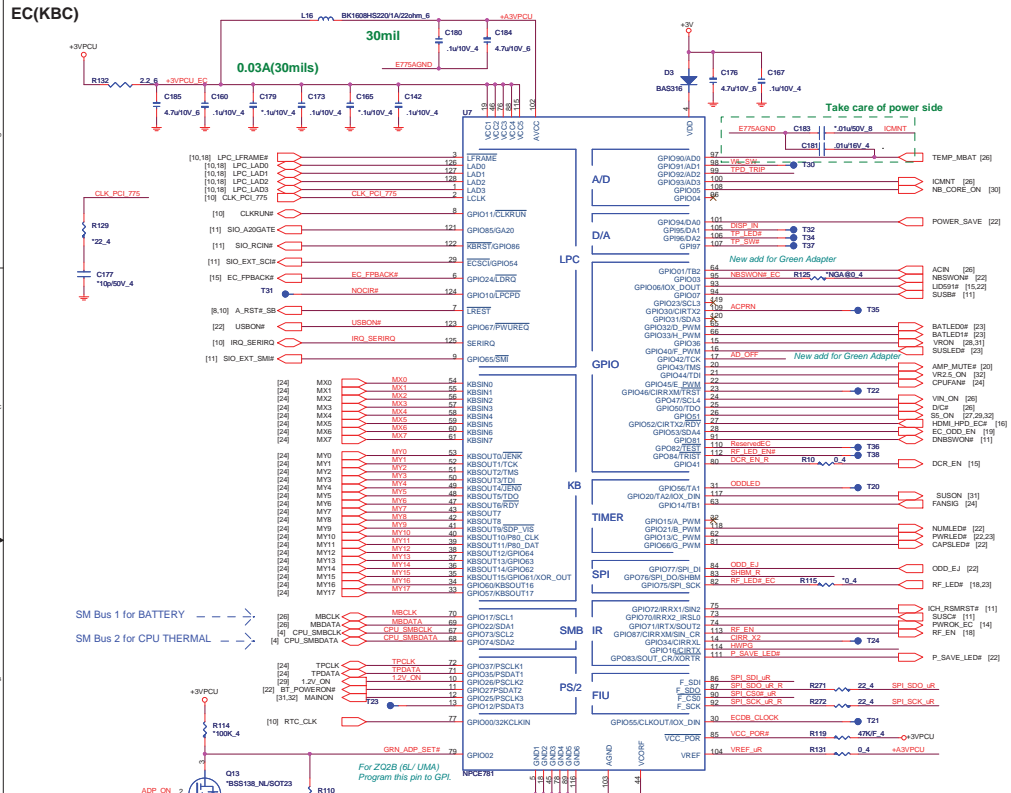
CPU FAN(THM)



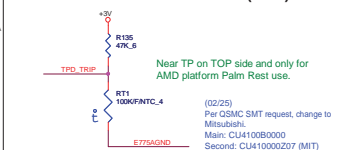
TOUCHPAD BOARD CONN(TPD)



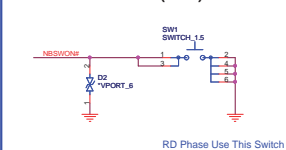
EC(KBC)



PALM REST THERMAL SENSOR (THM)



POWER-ON SWITCH (KBC)

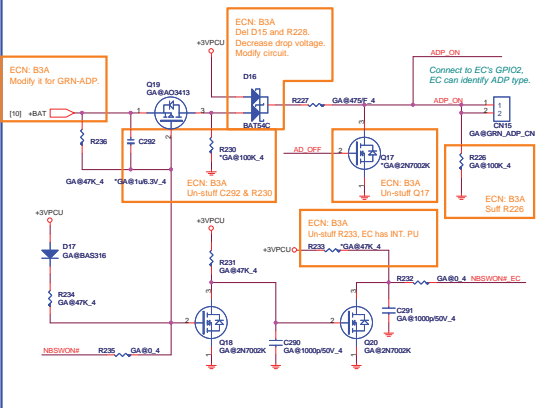


POWER-ON SWITCH (KBC)

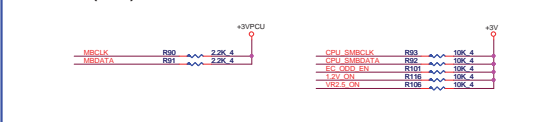
SHBM=0: Enable shared memory with host BIO

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

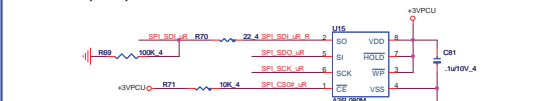
GREEN ADAPTER CIRCUIT



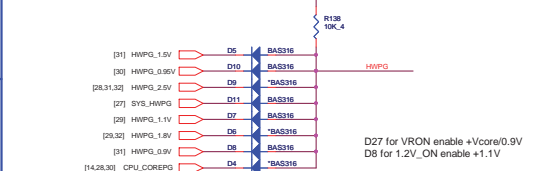
SM BUS PU(KBC)



SPI FLASH(KBC)

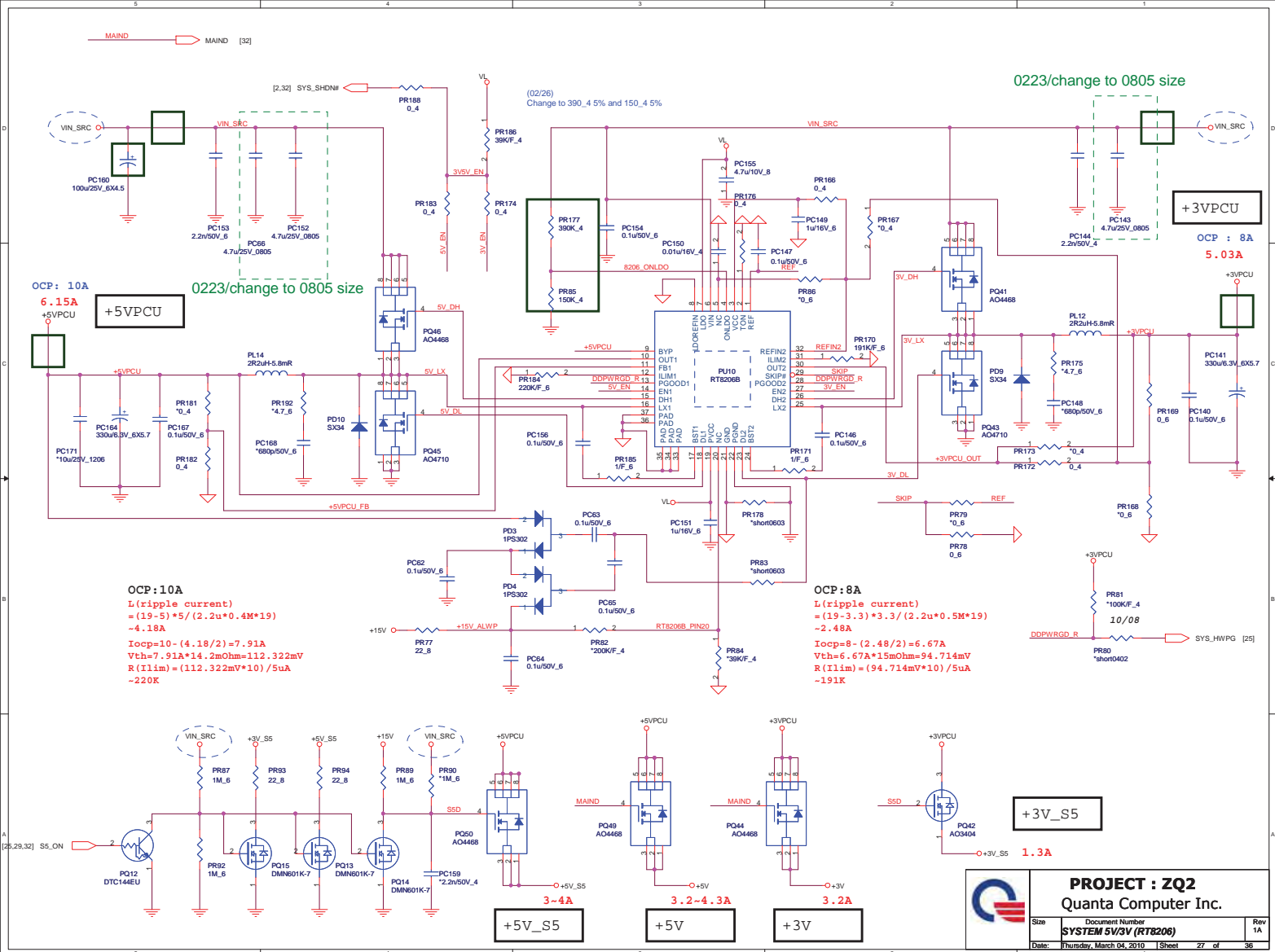


HWPG(KBC



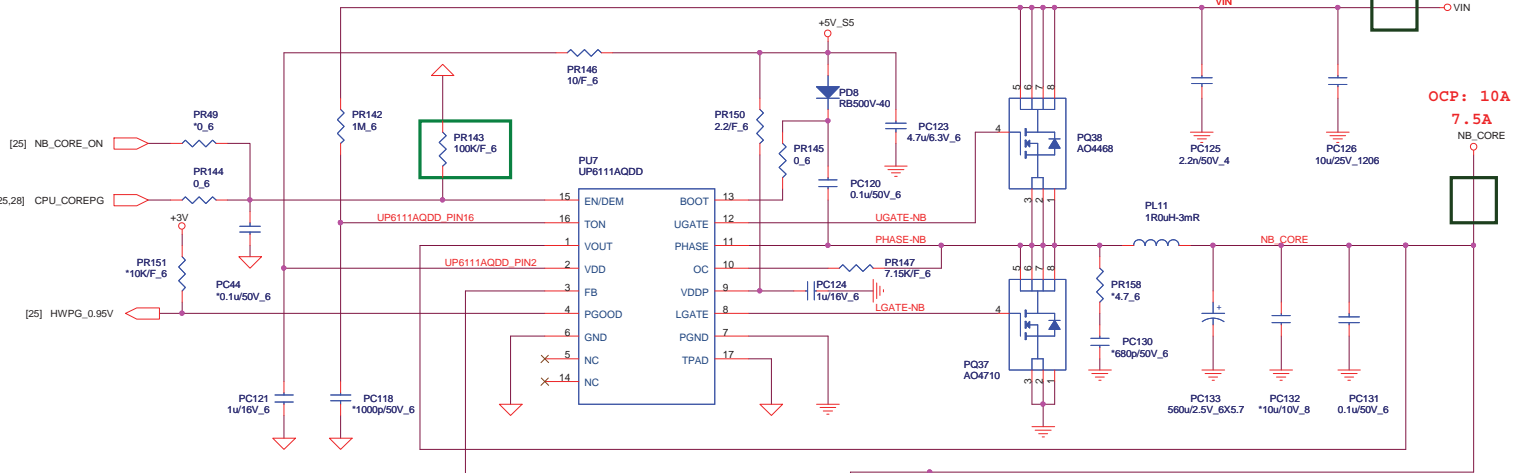
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SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8





$$VOUT = (1 + R1/R2) * 0.75$$

$$R_{ds} * OCP = RILIM * 20uA$$

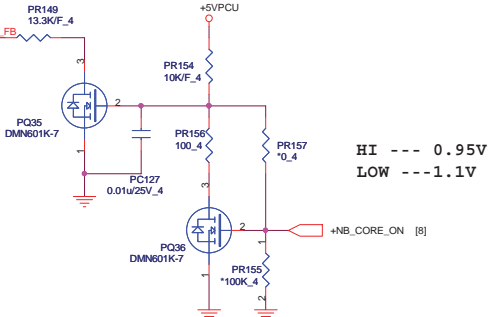
$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

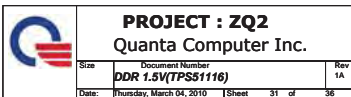
$$Frequency = 1 / (0.0036767) = 272K$$

AO4710 R_{ds(on)} = 11.7~14.2mOhm
 L(ripple current)
 = (19-1.05) * 1.05 / (1u * 272k * 19)
 ~3.646A
 14.2m * 10 = RILIM * 20uA
 RILIM = 7.1K --- 7.15K

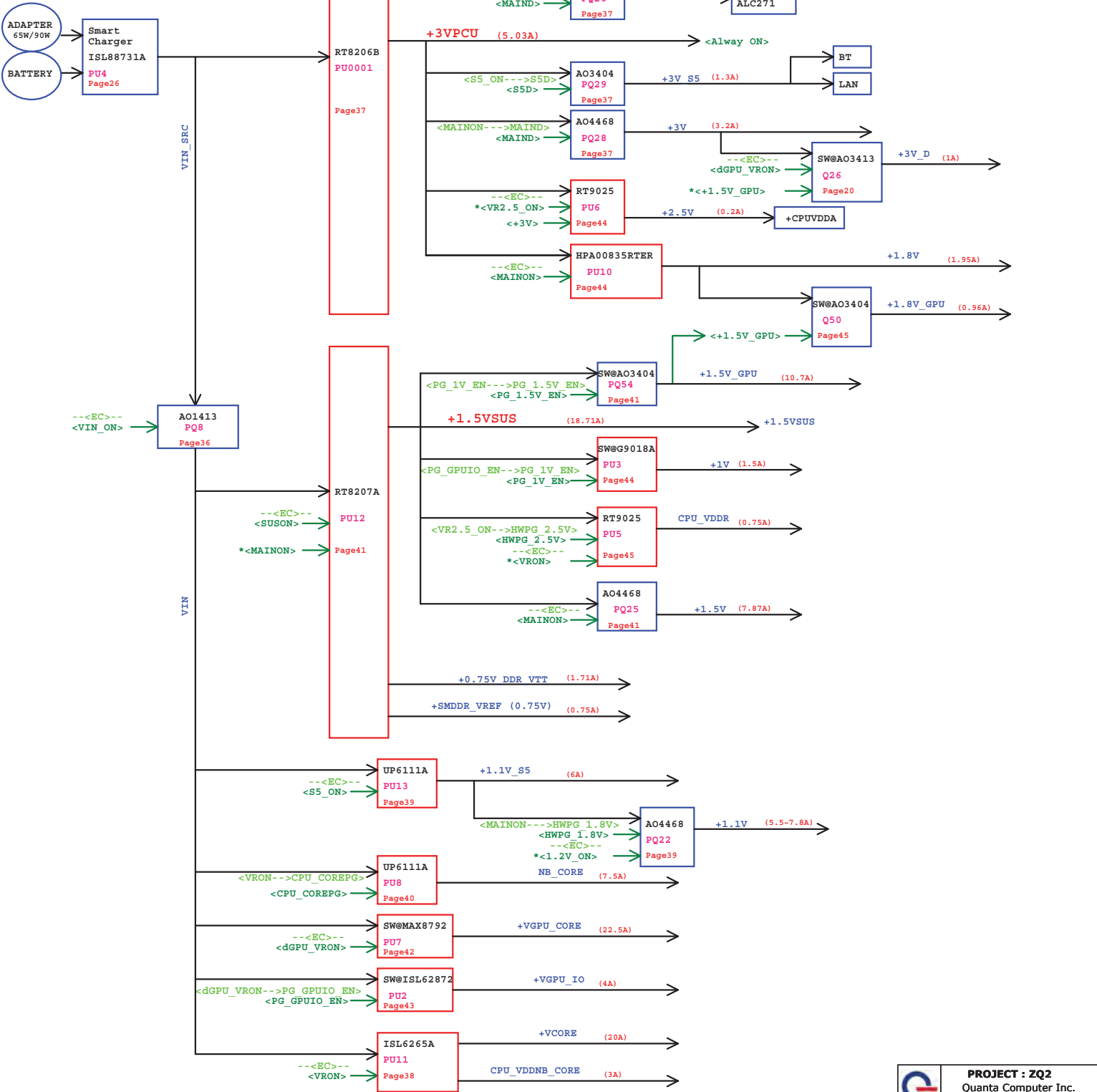


HI --- 0.95V
 LOW --- 1.1V

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ZQ2B Power tree



RS880:
1, $0 < (+3.3V) - (+1.8V) < 2.1$
2, +1.8V ramp before +1.1V
3, +1.1V ramp before VCC_NB



